REMARKS

This Amendment and Response is offered in reply to the Office Action mailed on December 5, 2006 and is filed subsequent to the Notice of Appeal and a Request for Pre-Appeal Brief Conference both filed on March 5, 2007. It is respectfully noted that this Amendment and Response is accompanied by a Request for Continued Examination.

No claims are amended; claims 1-3, 5-7, 9-12, 14-20, 22-26, 28-32, 34-38 and 40-51 are canceled; and claims 52-56 are added. As a result, claims 52-56 are now pending in this application.

§103 Rejection of the Claims

Claims 1-3 and 5-7 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Coad et al. (U.S. 6,851,107) in view of Takano (U.S. 6,591,152) in view of Pruitt (U.S. 6,179,490).

Claims 9-12, 14-20, 22-26, 28-32, 34-38 and 40-51 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Coad et al. in view of Takano (U.S. 6,591,152) to Gupta et al. (U.S. 5,825,651).

Applicant has chosen to cancel all of the previously pending claims to recast the focus on the patentable nature of the contributions of the present application in claims 52-56. Applicant reserves the right to reintroduce the cancelled claims at a later date and to submit further new claims. However, the reduced number of claims is intended to allow prosecution to be more focused in order to speed the prosecution process.

To help refocus prosecution of the present application, Applicant submits that the contributions of the present application allow a developer to quickly model and produce a semiconductor element, such as equipment, lot, wafer, die, etc. Such a model may be quickly made by selecting features to include, and to exclude, from a semiconductor element. Such features may be selected from a predefined group of features to form a feature diagram. As a result, the needs of a fabrication customer can be easily expressed in terms of features of a particular semiconductor element, and the semiconductor element quickly modeled.

Further, from the feature diagram, a statechart can be automatically modified as a function of the developer's feature selections. The statechart is then utilized to generate code which is executable within a controller of semiconductor fabrication equipment. That code may be deployed and executed within the semiconductor fabrication equipment to cause the semiconductor element to be fabricated.

Thus, the contributions of the present application include an end-to-end, modeling-to-fabrication solution to allow semiconductor elements to be rapidly produced.

To do so, as set forth in new independent claim 52, a developer may be presented with a group of predefined semiconductor element features in a feature diagram. The developer may then select features from this group for inclusion or exclusion from a semiconductor element. This allows a developer to move quickly from a requirement specification to a workable model. Further expediting the process is the manipulation of the statechart as a function of the received feature selections to generate a revised statechart. This happens automatically. Thus, once a developer is satisfied with the feature selections, the statechart is ready for use in the generation of computer executable code that can be executed to cause semiconductor fabrication equipment to fabricate the desired semiconductor element.

Selection of features for inclusion and exclusion, in the various embodiments set forth in the claims, is further aided by rules including or excluding other features based on selection of one or more other features. In addition, some features may be defined as default features. This allows a developer to select a minimal number of features for inclusion and exclusion and still be able to fabricate a functional semiconductor element.

Applicant respectfully submits that the new claims are patentable over the references used in the Final Office Action mailed December 5, 2006 because the cited references fail to teach or suggest each and every element in the claims.

For example, the group of predefined features are presented in a user interface as a feature model. The cited references do not provide such a feature model, let a lone a feature model from which to select features for inclusion or exclusion from a semiconductor element. Further, Applicant is unable to find a teaching of explicitly selecting a feature for exclusion from a semiconductor element. Also, the interaction between the feature diagram and the statechart is claimed, but not taught.

As previously argued, although statecharts may be shown in the cited references, there is no equivalent teaching of a feature diagram. For example, "The root of a feature diagram is a concept." Application, page 4, lines 26-27. A feature diagram is used at a high level to model concepts and concept features which are to be included in a system, rather than a system itself. Further insight into the composition of a feature diagram is provided in the application, such as at page 5, line 16 – page 6, line 30.

As a matter of contrast, the Office has previously asserted that Coad's component diagrams provide an equivalent teaching. However, Coad's component diagrams merely provide a static architectural view of a system or its component parts. *See* Coad, Col. 17, lines 34-43. This plainly does not include a concept as defined by the Applicant, and is not the same things as a feature diagram. Applicant therefore respectfully requests that the explicit static nature of the component diagram in Coad be considered within the context of the remainder of Coad's specification.

Further, the feature diagrams in newly added claim 52 are directly modified by the method. This also is not taught by the concept diagram of Coad because Coad describes a static architectural view, which includes the concept diagram. *See* Coad, Col. 17, lines 34-47. Thus, because the concept diagram is static, Applicant respectfully submits that "receiving, at the user interface, a selection of one or more features in the feature diagram to be included in or excluded from a semiconductor element" as set forth in claim 52 is not taught by Coad as previously asserted.

These deficiencies of the cited reference prevents the prior art from providing an end-to-end, modeling-to-fabrication solution to allow semiconductor elements to be produced rapidly. Elements of the present claims are involved in providing these advantages not found in the prior art. Thus, Applicant respectfully requests consideration and allowance of newly added claims 52-56.

Reservation of Rights

In the interest of clarity and brevity, Applicant may not have addressed every assertion made in the Office Action. Applicant's silence regarding any such assertion does not constitute any admission or acquiescence. Applicant reserves all rights not exercised in connection with this response, such as the right to challenge or rebut any tacit or explicit characterization of any reference or of any of the present claims, the right to challenge or rebut any asserted factual or legal basis of any of the rejections, the right to swear behind any cited reference such as provided under 37 C.F.R. § 1.131 or otherwise, or the right to assert co-ownership of any cited reference. Applicant does not admit that any of the cited references or any other references of record are relevant to the present claims, or that they constitute prior art. To the extent that any rejection or assertion is based upon the Examiner's personal knowledge, rather than any objective evidence of record as manifested by a cited prior art reference, Applicant timely objects to such reliance on Official Notice, and reserves all rights to request that the Examiner provide a reference or affidavit in support of such assertion, as required by MPEP § 2144.03. Applicant reserves all rights to pursue any cancelled claims in a subsequent patent application claiming the benefit of priority of the present patent application, and to request rejoinder of any withdrawn claim, as required by MPEP § 821.04.

CONCLUSION

The Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone the Applicant's attorney at (210) 308-5677 to facilitate prosecution of this application. If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Date May 7, 2007

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 7 day of May 2007.

Kate Gannon
Name

Signature